CLAIMS

We Claim:

1. A device to create, process and transfer packets of information from one device to another, comprising:

a plurality of micro-engines to receive payload data from a memory controller, determine if a task is available to process the payload data and assign a task to process the payload data;

a transmit cell FIFO circuit adapted to build a packet header based on payload data received from the plurality of micro-engines or directly from the memory controller and store payload data in a buffer, transmit the packet header with the payload data when all the payload data has been received and immediately begin to receive additional payload data from either the plurality of micro-engines or the memory controller when a predetermined amount of payload data has been transferred out of the buffer.

2. The device recited in claim 1, wherein the transmit cell FIFO further comprises:

a buffer control logic circuit adapted to receive packet data from the memory controller and place it in a cell buffer FIFO and begin transmitting to a destination when the packet header and packet data have been received.

3. The device recited in claim 2, wherein the buffer control logic circuit further comprises:

a address and write enable logic circuit to synchronize the receipt of the packet header from the plurality of micro-engines and the packet payload from the memory controller and place both the packet header and the packet payload into the cell buffer FIFO;

a cell buffer read logic circuit to transfer the packet header and packet payload data from the cell buffer FIFO to a destination specified by the packet header;

a cell buffer full logic circuit to signal the plurality of micro-engines and memory controller that a buffer is available to receive another packet header and another packet payload data when a predetermined amount of the packet header has been transferred by the cell buffer read logic circuit.

4. The device recited in claim 3, wherein the transmit cell FIFO circuit further comprises:

a cell buffer byte alignment circuit to track a start lane in the cell buffer FIFO indicating the start of free space in the cell buffer FIFO, determine a starting lane for the packet payload so that alignment of the payload data matches the start lane for the cell buffer FIFO.

5. The device recited in claim 4, wherein the cell buffer byte alignment circuit further comprises:

a byte counter circuit adapted to count a number of bytes that exist prior to a valid byte be found in the payload data;

a shift selector circuit to shift the payload data so that the first valid byte will match the first available space in the cell buffer FIFO; and

a data shift multiplexer to select between data received from the shift selector circuit or payload data received from a memory controller.

6. The device recited in claim 1, further comprising:

a sequencer adapted to identifying if a micro-engine task is available along with a dynamic cell buffer to process a request for receipt of a packet.

7. The device recited in claim 6, wherein the plurality of micro-engines further comprises:

a dynamic cell buffer circuit adapted to extracting a destination work queue from a packet header received from a transmitting device and signal the sequencer that a micro-engine task and dynamic cell buffer are to be assigned for the received packet.

8. The device recited in claim 7, wherein the plurality of micro-engines further comprises:

a cell byte register circuit to extract and opcode for the packet header, determine the number of bytes in the packet header, determine the total number of bytes in the packet payload and determine the number of bytes remaining in the dynamic cell buffer.

9. A device to receive packets of information from one device and transfer the packets to another device, comprising:

a plurality of micro-engines to receive a packet from a device, determine if a task is available to process the packet and assign a task and buffer to store the packet, said plurality of micro-engines further comprising:

a dynamic cell buffer circuit adapted to extract a destination work queue from a packet header contained in the packet received from a transmitting device and signal a sequencer that a micro-engine task and dynamic cell buffer are to be assigned for the received packet; and

a cell byte register circuit to extract an opcode for the packet header, determine the number of bytes in the packet header, determine the total number of bytes in the packet payload and determine the number of bytes remaining in the dynamic cell buffer.

10. The device recited in claim 9, wherein the dynamic cell buffer circuit further comprises:

a data snooper and control logic circuit adapted to receiving the packet from the device and transmit a request that a micro-engine task be assigned to process the packet.

11. The device recited in claim 10, further comprising

a sequencer adapted to receive the request that a micro-engine task be assigned to process the packet, to identify if a micro-engine task is available to process to packet, and assign a micro-engine task and a dynamic cell buffer to the packet.

12. The device recited in claim 11, wherein the dynamic cell buffer circuit further comprises:

a request counter to count the number of packets received by the data snooper and control logic circuit and transmit the count to the sequencer; and

a work queue request order FIFO connected to the data snooper and control logic to receive a destination work queue number extracted by the data snooper and control logic and transmit the work queue number to the sequencer..

13. The device recited in claim 12, wherein the dynamic cell buffer circuit further comprises:

a buffer request order FIFO circuit connected to the data snooper and control logic circuit to identify a dynamic cell buffer of a plurality of dynamic cell buffers and assign a dynamic cell buffer to the work queue number for the packet; and

a valid and task control circuit to set a valid bit in the assigned dynamic cell buffer upon receipt of an acknowledgement from the sequencer.

14. The device recited in claim 9, wherein cell byte register circuit further comprises:

and opcode decoder circuit adapted to identifying the opcode in the packet header and determine based upon the opcode the length of the packet header.

15. The device recited in claim 14, wherein cell byte register circuit further comprises:

a subtractor circuit adapted to determining a payload length by subtracting the length of the packet header from an entire length of a packet; and

a cell bytes remaining register adapted to subtracting a number of bytes transferred from the dynamic cell buffer from the payload length.

16. A device to create and transmit packets of data, comprising:

a transmit cell FIFO circuit adapted to build a packet header based on payload data received from a plurality of micro-engines or directly from a memory controller, said transmit cell FIFO circuit further comprising:

a buffer control logic circuit adapted to receive packet data from the memory controller or the plurality of micro-engines and place it in a cell buffer FIFO and begin transmitting to a destination when a packet header and payload data have been received; and

a cell buffer byte alignment circuit to track a start lane in the cell buffer FIFO indicating the start of free space in the cell buffer FIFO, to determine a starting lane for alignment of the packet payload matches the start lane for the cell buffer FIFO .

17. The device recited in claim 16, wherein the buffer control logic circuit further comprises:

a address and write enable logic circuit to synchronize the receipt of the packet header from the plurality of micro-engines and the packet payload from the memory controller and place both the packet header and the packet payload into the cell buffer FIFO;

a cell buffer read logic circuit to transfer the packet header and packet payload data from the cell buffer FIFO to a destination specified by the packet header;

a cell buffer full logic circuit to signal the plurality of micro-engines and memory controller that a buffer is available to receive another packet header and another packet payload data when a predetermined amount of the packet header has been transferred by the cell buffer read logic circuit.

18. The device recited in claim 16, wherein the cell buffer byte alignment circuit further comprises:

a byte counter circuit adapted to count a number of bytes that exist prior to a valid byte be found in the payload data;

a shift selector circuit to shift the payload data so that the first valid byte will match the first available space in the cell buffer FIFO; and

a data are shift multiplexer to select between data received from the shift selector circuit or payload data received from a memory controller.